SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

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Kawasaki, Japan, Tatsuo Koizumi, a citizen of Japan residing
at Kawasaki, Japan have invented certain new and useful
improvements in

NOISE COUNTERMEASURE DETERMINATION METHOD AND
APPARATUS AND STORAGE MEDIUM

of which the following is a specification : -

TITLE OF THE INVENTION
NOISE COUNTERMEASURE DETERMINATION METHOD
AND APPARATUS AND STORAGE MEDIUM

5 BACKGROUND OF THE INVENTION

This application claims the benefit of a
Japanese Patent Applications No.2000-138681 filed
May 11, 2000 and No.2000-159100 filed May 29, 2000,
in the Japanese Patent Office, the disclosures of

10 which are hereby incorporated by reference.

1. Field of the Invention

The present invention generally relates to
noise countermeasure determination methods and
apparatuses and storage media, and more particularly

15 to a noise countermeasure determination method which
determines noise countermeasures for guaranteeing a
normal operation of an electronic circuit by
minimizing noise which may be generated in the
electronic circuit when designing the electronic

20 circuit such as a large scale integrated (LSI)
circuit, multi-chip module (MCM) and printed circuit
board (PCB), and to a noise countermeasure
determination apparatus which determines the noise
countermeasures by such a noise countermeasure

25 determination method, and to a computer-readable
storage medium which stores a program for causing a
computer to carry out such a noise countermeasure
determination.

Recently, the noise countermeasures and

30 noise analysis have become important when designing
the electronic circuit, particularly because the
size of electronic circuits has decreased
considerably and the operation speed of the
electronic circuits has increased greatly. The

35 noise countermeasures refer to various measures
which are taken to suppress the noise generated in
the electronic circuit, based on results obtained by

the noise analysis.

2.   Description of the Related Art

Conventionally, various kinds of noise analyzing tools have been proposed to carry out the noise analysis when designing the electronic circuit. The noise analyzing tool carries out the noise analysis and a noise check using a circuit simulator after an assemble design of the electronic circuit is made, so as to determine noise countermeasures for suppressing the noise. The design of the electronic circuit is modified if necessary based on the determined noise countermeasures. After such a design modification, the noise analysis and the noise check are carried out again, and the above described procedure is repeated until the noise falls within a tolerable range.

The noise which is to be mainly considered when designing the electronic circuit includes reflection noise and crosstalk noise. Normally, the reflection noise is generated by a mismatch of an internal resistance of a driver and a characteristic impedance of a transmission line. In order to suppress the reflection noise, a method has been proposed to insert a damping resistor in series to an output of the driver particularly in the case of a 1:1 transmission. According to this proposed method, a resistance of the damping resistor is selected so that a sum of the internal resistance of the driver and the damping resistance becomes equal to the characteristic impedance of the transmission line.

The reflection noise in transmissions other than the 1:1 transmission, such as a 1:N transmission, greatly depends on the wiring (or routing) topology. For this reason, the wiring topology is selected manually, so as to carry out the wiring to suit the wiring topology selected by

the designer. Accordingly, the circuit simulator carries out the noise analysis and the noise check based on the wiring information. If noise exceeding a tolerable range exists as a result of the noise

5 analysis, operations such as a modification of the wiring topology, a rewiring to suit the wiring topology, a noise analysis and a noise check are repeated so as to find an optimum wiring topology.

On the other hand, the crosstalk noise

10 greatly depends on the driving capacity of the driver, a gap between adjacent patterns, and the like. Usually, the crosstalk analysis requires information related to the adjacent patterns, and for this reason, the noise analysis and the noise

15 check are carried out after the assemble design of the electronic circuit is made, using assemble design data. The information related to the adjacent patterns include a pattern gap, a distance for which the patterns run parallel to each other, a

20 position where the patterns are parallel on the transmission lines, and the like.

However, due to the further size reduction and the further increased operation speed of recent electronic circuits, the number of nets which

25 require the noise analysis and the noise check is increasing, thereby increasing the number of design steps. A net refers to a part which is made up of at least one target circuit element when designing the electronic circuit. For this reason, it is

30 necessary to take noise countermeasures not requiring a backward process which is a repetition of manual operations including circuit design, assemble design and noise analysis. In other words, prior to the circuit design and the assemble design,

35 it is necessary to create a circuit model amounting to at least one net, so as to determine the noise countermeasures based on the circuit model input.

But even in a case where the circuit model amounting to at least one net is created and the noise analysis and the noise countermeasures are carried out, before the circuit design and the

5 assemble design, a processing time as a whole becomes considerably long if the noise countermeasures are always determined by the circuit simulator, since a processing time of the circuit simulator is long compared to other processes.

10 Consequently, the problem of the considerably long processing time of the circuit simulator becomes particularly conspicuous when repeating operation cycles such as design, analysis, countermeasures (design modification) and analysis. For this reason,

15 there were demands to determine the noise countermeasures by suppressing the operation of the circuit simulator to a minimum.

In order to suppress the operation of the circuit simulator to a minimum, it is necessary to

20 select the damping resistance without using the results of the circuit simulator, even for the countermeasures against the reflection noise. However, if the damping resistance which matches the output resistance of the driver element and the

25 characteristic impedance of the wiring is used as the recommended circuit information, this damping resistance will not match the damping resistance which is already inserted in the input circuit information, even though a problem will not occur in

30 the actual transmission waveform. As a result, there was a problem in that the noise countermeasures which are determined in such a case may be too severe and require the damping resistor to be modified.

35 In addition, when determining the wiring topology, it is necessary to repeat the wiring topology selection, wiring modification and noise

analysis. But if the wiring topology selection and the wiring modification are to be made by the designer, there was a problem in that it takes too long to carry out such operations manually. For this reason, there were demands to repeat the wiring topology selection, wiring modification and noise analysis within a short time, and to determine the noise countermeasures by selecting an optimum wiring topology.

Furthermore, according to the crosstalk noise analyzing method described above, the noise analysis and the noise check are made using the design data after the assemble design. Accordingly, when the crosstalk noise is found as a result of the noise check, it is necessary to modify the assemble design, and the design steps need to include a backward process which repeat manual operations. Consequently, there were demands to reduce the design steps by eliminating the backward process which repeat manual operations.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide a novel and useful noise countermeasure determination method and apparatus and computer-readable storage medium, in which the problems described above are eliminated.

A first object of the present invention is to provide a noise countermeasure determination method and apparatus and computer-readable storage medium which can determine. noise countermeasures before a circuit design and an assemble design, and suppress an operation of a circuit simulator to a minimum when determining the noise countermeasures, so that the noise countermeasures can be determined at a high speed without generating in design steps a backward process which is a repetition of manual

operations.

A second object of the present invention is to provide a noise countermeasure determination method and apparatus and computer-readable storage

5 medium which can determine a damping resistance without the need to carry out an operation of a circuit simulator and without making the noise countermeasures too severe.

A third object of the present invention is

10 to provide a noise countermeasure determination method and apparatus and computer-readable storage medium which can determine an optimum wiring topology from relative positional relationships on an actual printed circuit board or the like, prior

15 to a circuit design and an assemble design.

A fourth object of the present invention is to provide a noise countermeasure determination method and apparatus and computer-readable storage medium which can determine noise countermeasures by

20 taking crosstalk noise into consideration, by analyzing the crosstalk noise prior to a circuit design and an assemble design.

Another and more specific object of the present invention is to provide a noise

25 countermeasure determination method and apparatus and computer-readable storage medium, which can suppress the operation of a circuit simulator to a minimum when determining noise countermeasures, so that the noise countermeasures can be determined at

30 a high speed without generating in the design steps a portion which requires a backward process which is a repetition of manual operations.

Still another object of the present invention is to provide a noise countermeasure

35 determination method comprising the steps of (a) calculating recommended circuit information considered to minimize a noise by use of at least

one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis, and (b) comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures. According to the noise countermeasure determination method of the present invention, it is possible to realize the first object described above.

The noise countermeasure determination method may further comprise the steps of (c) creating a simulation model of the input circuit information after determining the noise countermeasures in the step (b), (d) carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform, and (e) categorizing the noise existing as a result of the noise check carried out in the step (d), and optimizing the determined noise countermeasures to only portions related to the noise. According to the noise countermeasure determination method of the present invention, it is possible to realize the second object described above.

The noise countermeasure determination method may further comprises the step of (c) outputting input circuit information which includes as, a wiring length, a Manhattan distance which is determined based on positions of part pins forming the target circuit and a wiring topology. According to the noise countermeasure determination method, it is possible to realize the third object described above.

The noise countermeasure determination method may further comprise the steps of (c) creating a simulation model of input circuit information made up of circuit information of a

5   target net which is to be subjected to the noise analysis and circuit information of an adjacent net which is adjacent to the target net, after determining the noise countermeasures in the step (b), (d) carrying out a circuit simulation using the

10   simulation model, to obtain a noise combined waveform by combining a crosstalk noise waveform and a signal waveform propagating through the target net which are calculated, and to check whether or not a noise exceeding a tolerable range exists based on

15   the noise combined waveform, and (e) categorizing the noise existing as a result of the noise check carried out in the step (d), and optimizing the determined noise countermeasures to only portions related to the noise. According to the noise

20   countermeasure determination method of the present invention, it is possible to realize the fourth object described above.

A further object of the present invention is to provide a noise countermeasure determination

25   apparatus comprising a recommended circuit information calculating section calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at

30   least one net of a target circuit which is to be subjected to a noise analysis, and a noise countermeasure determination section comparing the input circuit information and the recommended circuit information, and determining a differing

35   portion of the recommended circuit information differing from the input circuit information, as noise countermeasures. According to the noise

countermeasure determination apparatus of the preset invention, it is possible to realize the first object described above.

Another object of the present invention is to provide a computer-readable storage medium which stores a program for causing a computer to determine noise countermeasures, where the program comprises a recommended circuit information calculating procedure causing the computer to calculate recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis, and a noise countermeasure determination procedure causing the computer to compare the input circuit information and the recommended circuit information, and to determine a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures. According to the computer-readable storage medium of the present invention, it is possible to realize the first object described above.

Therefore, according to the present invention, it is possible to realize a noise countermeasure determination method and apparatus and computer-readable storage medium, which can suppress the operation of a circuit simulator to a minimum when determining noise countermeasures, so that the noise countermeasures can be determined at a high speed without generating in the design steps a portion which requires a backward process which is a repetition of manual operations.

Other objects and further features of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view showing a computer system applied with the present invention in a first embodiment of the present invention;

FIG. 2 is a system block diagram for explaining a construction of an important part within a main body of the computer system;

FIG. 3 is a flow chart for explaining a noise countermeasure determination process of a CPU in the first embodiment;

FIG. 4 is a flow chart for explaining a noise countermeasure determination process of the CPU in a second embodiment of the present invention;

FIG. 5 is a diagram for explaining input circuit information;

FIG. 6 is a diagram showing a relationship of a first rising voltage, and a maximum voltage and a minimum voltage of a circuit;

FIG. 7 is a diagram for explaining a relationship of the voltage and the minimum voltage of the circuit at a time of a ringback;

FIG. 8 is a flow chart for explaining a noise countermeasure determination process of the CPU in a third embodiment of the present invention;

FIG. 9 is a diagram showing a case where placement positions of input/output buffers are input without routing of wirings;

FIG. 10 is a flow chart for explaining a noise countermeasure determination process of the CPU in a fourth embodiment of the present invention;

FIG. 11 is a flow chart for explaining a noise countermeasure determination process of the CPU in a fifth embodiment of the present invention;

FIG. 12 is a diagram for explaining circuit information of a target net and an adjacent net;

FIG. 13 is a flow chart for explaining a noise countermeasure determination process of the CPU in a sixth embodiment of the present invention;

FIG. 14 is a diagram for explaining circuit information of a target net and an adjacent net;

FIG. 15 is a flow chart for explaining a noise countermeasure determination process of the CPU in a seventh embodiment of the present invention;

FIG. 16 is a diagram showing input circuit information;

FIG. 17 is a diagram showing recommended circuit information with respect to the input circuit information shown in FIG. 16;

FIG. 18 is a diagram showing input circuit information;

FIG. 19 is a diagram for explaining recommended circuit information with respect to the input circuit information shown in FIG. 18;

FIG. 20 is a diagram showing input circuit information;

FIG. 21 is a diagram for explaining recommended circuit information with respect to the input circuit information shown in FIG. 20;

FIG. 22 is a flow chart for explaining a noise countermeasure determination process of the CPU in an eighth embodiment of the present invention;

FIG. 23 is a flow chart for explaining a noise countermeasure determination process of the CPU in a ninth embodiment of the present invention;

FIG. 24 is a diagram showing a load concentration type wiring topology for a unidirectional transmission;

FIGS. 25A and 25B respectively are diagrams showing a star type wiring topology for the

unidirectional transmission; and

FIGS. 26A and 26B respectively are diagrams showing a daisy chain type wiring topology for the unidirectional transmission.

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DESCRIPTION OF THE PREFERRED EMBODIMENTS

A description will be given of various embodiments of a noise countermeasure determination method, a noise countermeasure determination

10 apparatus and a computer-readable storage medium according to the present invention, by referring to the drawings.

First, a description will be given of a first embodiment of the noise countermeasure

15 determination apparatus according to the present invention. This first embodiment of the noise countermeasure determination apparatus employs a first embodiment of the noise countermeasure determination method according to the present

20 invention and a first embodiment of the computer-readable storage medium according to the present invention. In this first embodiment, the present invention is applied to a computer system. FIG. 1 is a perspective view showing the computer system to

25 which the present invention is applied in this first embodiment. It is assumed for the sake of convenience that the computer system shown in FIG. 1 is also used in each of second and subsequent embodiments which will be described later.

30 A computer system 100 shown in FIG. 1 is generally provided with a main body 101 which includes a CPU, a disk drive and the like, a display 102 which includes a display screen 102a for displaying an image in response to an instruction

35 from the main body 101, a keyboard 103 which is used to input various information to the computer system 100, a mouse 104 which is used to specify an

arbitrary position on the display screen 102a of the display 102, and a modem 105 which is used to access an external database or the like and to download programs or the like stored in another computer

5   system.

A noise countermeasure determination program (or a noise countermeasure determination software) which causes the computer system 100 to have a noise countermeasure determination function

10   is stored in a portable recording medium such as a disk 110 or, is downloaded from a recording medium 106 of another computer system using a communication unit such as the modem 105. The computer-readable storage medium according to the present invention is

15   formed by a recording medium, such as the disk 110, which stores the noise countermeasure determination program. The recording medium forming the computer-readable storage medium according to the present invention is not limited to portable recording media

20   such as the disk 110, IC card memory, floppy disk, magneto-optical disk and CD-ROM, but also includes various kinds of recording media which are accessible by a computer system which is coupled via the communication unit or communication means such

25   as the modem 105 and LAN.

FIG. 3 is a system block diagram for explaining the structure of an important part within the main body 101 of the computer system 100. In FIG. 3, the main body 101 generally includes a CPU

30   201, a memory part 202 made of RAM, ROM or the like, a disk drive 203 for the disk 110, and a hard disk drive (HDD) 204 which are connected via a bus 200. The display 102, the keyboard 103, the mouse 104 and the like may be connected to the CPU 201 via the bus

35   200 as shown in FIG. 3 or, connected directly to the CPU 201. It is also possible to connect the display 102 to the CPU 201 via a known graphic interface

(not shown) which carries out an input/output image data processing.

Of course, the structure of the computer system 100 is not limited to that shown in FIGS. 1 and 2, and various other known structures may be used instead.

FIG. 3 is a flow chart for explaining a noise countermeasure determination process of the CPU 201 in this first embodiment. In this embodiment, noise countermeasures are determined without the use of a circuit simulator, before a circuit design and an assemble design of a target electronic circuit are made. In FIG. 3, when the noise countermeasure determination process is started, a step 1 inputs input circuit information amounting to at least one net of a target electronic circuit from the keyboard 103 or an external unit. A step 2 stores the input circuit information in a storage means such as the memory part 202. A step 3 calculates recommended circuit information which is considered to minimize noise using at least one calculation formula, based on the input circuit information read from the memory part 202. The recommended circuit information includes a damping resistance, a wiring length between a driver and a resistor, a wiring length between a resistor and a receiver, a position of a wiring branching point, a wiring length between a resistor and a branching point, a wiring length between a branching point and a receiver, a driving capacity of a driver, a number of loads (receivers), and the like. A step 4 stores the calculated recommended circuit information in a storage means such as the memory part 202. A step 5 compares the input circuit information and the recommended circuit information read from the memory part 202, and determines differing portions of the recommended circuit

information as noise countermeasures. A step 6
outputs the determined noise countermeasures by
displaying the noise countermeasures on the display
102, for example.

5   FIG. 4 is a flow chart for explaining a
noise countermeasure determination process of the
CPU 201 of the computer system 100 which is applied
with a second embodiment of the noise countermeasure
determination method, a second embodiment of the
10   noise countermeasure determination apparatus and a
second embodiment of the computer-readable storage
medium according to the present invention. In FIG.
4, those steps which are the same as those
corresponding steps in FIG. 3 are designated by the
15   same reference numerals, and a description thereof
will be omitted. In this second embodiment, the
noise countermeasures determined by the first
embodiment described above are further optimized
using analysis results of a circuit simulator, so as
20   to determine more restricted noise countermeasures.

In FIG. 4, a step 7 creates a circuit mode,
that is, a simulation model, based on the noise
countermeasures obtained by the step 5. A step 8
analyzes the created circuit model using a circuit
25   simulator. A step 9 checks whether or not a noise
which cause problems, that is, a noise exceeding a
tolerable range, is generated, based on the analysis
results of the circuit simulator. The noise check
is made by detecting the noise existing in a signal
30   waveform propagating through a wiring of the
electronic circuit, for example, which signal
waveform is output from the circuit simulator. A
step 10 categorizes results of the noise check, and
restricts the noise countermeasures output by the
35   step 6 to only portions related to the categorized
results of the noise check. A step 11 outputs the
restricted noise countermeasures by displaying the

restricted noise countermeasures on the display 102,
for example.

According to the first and second
embodiments described above, it is possible to
5   determine the noise countermeasures before the
circuit design and the assemble design of the target
electronic circuit, by inputting the circuit
information amounting to at least one net. In
addition, by obtaining the recommended circuit
10   information based on the at least one calculation
formula, it is possible to determine the noise
countermeasures by suppressing the operation of the
circuit simulator to a minimum as in the second
embodiment.

15   In the second embodiment, the input
circuit information which is input in the step 1 is,
for example, information amounting to one net shown
in FIG. 5. The input circuit information shown in
FIG. 5 includes a driver with a resistance R0 = 20
20   Ohms (Ω), a wiring having a wiring length L = 20 mm
and an impedance Z0 = 60 Ohms, a resistor having a
resistance Rs = 20 Ohms, a wiring having a wiring
length L = 20 mm and an impedance Z0 = 60 Ohms, and
a receiver. In this case, a clock frequency of the
25   net, a delay between pins, a signal propagation
speed on a pattern, a layer structure, a pattern
width and the like may be input in addition to the
input circuit information shown in FIG. 5.

The step 3 obtains the recommended circuit
30   information which is considered to minimize the
noise using the at least one calculation formula,
based on the input circuit information. It will be
assumed for the sake of convenience that the
recommended circuit information which is obtained
35   based on the input circuit information shown in FIG.
5 includes a damping resistance. For example, when
the step 8 calculates based on the input circuit

information shown in FIG. 5 that a damping
resistance at which a first rising voltage of an
input waveform matches a maximum voltage VIH-2 which
guarantees a normal operation of the circuit is 12

5   Ohms, and a damping resistance at which the first
rising voltage of the input waveform matches a
minimum voltage VIH-1 which guarantees the normal
operation of the circuit is 67 Ohms, the damping
resistance of the recommended circuit information

10   becomes 12 to 67 Ohms.

FIG. 6 is a diagram showing a relationship
of the first rising voltage, and the maximum voltage
VIH-2 and the minimum voltage VIH-1 of the circuit.
In FIG. 6, the ordinate indicates the voltage, and

15   the abscissa indicates the time. In this case, the
step 5 obtains, as the noise countermeasures, a
damping resistance which makes the first rising
voltage indicated by a dotted line in FIG. 6 to fall
within a range less than or equal to the maximum

20   voltage VIH-2 and greater than or equal to the
minimum voltage VIH-1. In other words, because the
damping resistance of the input circuit information
is 10 Ohms and the damping resistance of the
recommended circuit information is 12 to 67 Ohms,

25   the step 5 compares the damping resistances and
determines the noise countermeasures as being to
modify the damping resistance of the input circuit
information to the damping resistance of the
recommended circuit information, which is 12 to 67

30   Ohms.

When calculating the damping resistance
based on the input circuit information shown in FIG.
5, it is possible to take into consideration a
voltage at the time of a ringback. It is assumed

35   for the sake of convenience that a damping
resistance at which the voltage at the time of the
ringback matches the minimum voltage VIH-1 of the

circuit is calculated to be 14 Ohms. In this case,
a damping resistance at which the first rising
voltage of the input waveform matches the maximum
rated voltage of the circuit is 12 Ohms, but the

5   damping resistance of 14 Ohms at the time of the
ringback is used as a minimum value of the damping
resistance. Hence, the damping resistance of the
recommended circuit information becomes 14 to 67
Ohms. FIG. 7 is a diagram showing a relationship of

10   the voltage at the time of the ringback and the
minimum voltage VIH-1 of the circuit. In FIG. 7,
the ordinate indicates the voltage, and the abscissa
indicates the time. Accordingly, the noise
countermeasures, that is, the damping resistance,

15   are determined in this case so that in addition to
the first rising voltage, the voltage at the time of
the ringback indicated by a dotted line in FIG. 7
falls within a range greater than or equal to the
minimum voltage VIH-1 of the circuit.

20   FIG. 8 is a flow chart for explaining a
noise countermeasure determination process of the
CPU 201 of the computer system 100 which is applied
with a third embodiment of the noise countermeasure
determination method, a third embodiment of the

25   noise countermeasure determination apparatus and a
third embodiment of the computer-readable storage
medium according to the present invention. In FIG.
8, those steps which are the same as those
corresponding steps in FIG. 4 are designated by the

30   same reference numerals, and a description thereof
will be omitted. In order to omit input of routing
and wiring length information when inputting the
input circuit information, this third embodiment
inputs positions of part pins such as input/output

35   (I/O) buffers forming the circuit, and uses a
Manhattan distance which is obtained from the
positions of the part pins and the wiring topology,

as the wiring length.

In FIG. 8, in order to omit the input of the routing and wiring length information, the step 1 inputs the positions of the part pins forming the

5   circuit, that is, the placement positions, as the input circuit information. Hence, a step 13 stores the placement positions, as the input circuit information, in a storage means such as the memory part 202. A step 15 calculates, as the wiring

10   length, the Manhattan distance or a provisional wiring length based on the placement positions which are read from the memory part 202 as the input circuit information and the specified wiring topology. A step 16 stores the calculated wiring

15   length, as the circuit information, in a storage means such as the memory part 202. Hence, the step 3 in this embodiment calculates the recommended circuit information based on the wiring length, that is, the Manhattan distance.

20   Next, a description will be given of a case where the Manhattan distance which is obtained from the placement positions of the input/output buffers and the wiring topology, as the wiring length. FIG. 9 is a diagram showing a case where

25   the placement positions of the input/output buffers are input without routing of the wirings. In FIG. 9, coordinates indicated in brackets indicate placement positions of the input/output buffers. In this case, an output buffer (driver) is placed at the

30   coordinate (15, 90), and an input buffer (receiver) is placed at each of the coordinates (120, 50) and (95, 175). When a "star type" wiring topology is specified, the step 15 first calculates the position of a branching point as being (20, 95) so as to suit

35   the wiring topology. In other words, since the specified wiring topology is the "star type", the position of the branching point is determined so

that the Manhattan distance from the branching point
to the receiver becomes the same for the two
receivers and the distance from the driver to the
branching point becomes as short as possible. In
5   the case shown in FIG. 9, the wiring length from the
driver to the branching point is calculated as being
15 mm, and the wiring length from the driver to each
of the two receivers is calculated as being 150 mm,
from the Manhattan distance, when the units of the
10   coordinates are regarded as being in mm. Thereafter,
these wiring lengths are used as the wiring length
of the input circuit information.

In a modification, the wiring topology is
not specified, the selectable wiring topologies are
15   defined in advance, and the wiring length is
calculated from the Manhattan distance by
successively changing the wiring topology. In this
case, the selectable wiring topologies may include
the "star type", "load concentration type", "daisy
20   chain" type, "H-type" and the like.

FIG. 10 is a flow chart for explaining a
noise countermeasure determination process of the
CPU 201 of the computer system 100 which is applied
with a fourth embodiment of the noise countermeasure
25   determination method, a fourth embodiment of the
noise countermeasure determination apparatus and a
fourth embodiment of the computer-readable storage
medium according to the present invention. In FIG.
10, those steps which are the same as those
30   corresponding steps in FIG. 8 are designated by the
same reference numerals, and a description thereof
will be omitted. In this fourth embodiment, the
wiring topology is not specified, and the processes
up to the noise check are repeated using all
35   selectable wiring topologies, so as to determine an
optimum wiring topology from the results of the
noise check.

In FIG. 10, the step 15 calculates, as the
wiring length, the Manhattan distance based on the
placement positions read from the memory part 202 as
the input circuit information and a first wiring
topology of the selectable wiring topologies. A
step 9-1 carries out a noise check, and decides
whether or not a selectable wiring topology remains.
The process returns to the step 15 if the decision
result in the step 9-1 is YES. Hence, the steps 15,
16, 7, 8 and 9-1 are repeated until no more
selectable wiring topology remains and the decision
result in the step 9-1 becomes NO. As a result, a
step 17 obtains the optimum wiring topology as the
noise countermeasures, based on the results of the
repeated noise checks, and a step 18 outputs the
optimum wiring topology which is obtained.

FIG. 11 is a flow chart for explaining a
noise countermeasure determination process of the
CPU 201 of the computer system 100 which is applied
with a fifth embodiment of the noise countermeasure
determination method, a fifth embodiment of the
noise countermeasure determination apparatus and a
fifth embodiment of the computer-readable storage
medium according to the present invention. In FIG.
11, those steps which are the same as those
corresponding steps in FIG. 8 are designated by the
same reference numerals, and a description thereof
will be omitted. In this fifth embodiment, the
noise check which is carried out takes into
consideration a crosstalk noise.

In FIG. 11, of the input circuit
information input by the step 1, circuit information
related to a target net which is the target of the
analysis is stored in a storage means such as the
memory part 202 in the step 2, and the circuit
information related to an adjacent net which is
adjacent to the target net is stored in a storage

means such as the memory part 202 in a step 19. A
step 7-1 creates a simulation model of the target
net and the adjacent net. Accordingly, the step 19
carries out a circuit simulation based on this
5   simulation model, to calculate a propagation signal
waveform and a crosstalk noise waveform of the
target net, and to obtain a noise combined waveform
by combining the propagation signal waveform and the
crosstalk noise waveform. In addition, the step 9
10   carries out a noise check based on the noise
combined waveform.

FIG. 12 is a diagram for explaining
circuit information of the target net and the
adjacent net. As shown in FIG. 12, a crosstalk
15   portion which should consider the crosstalk is
specified within the net, and a pattern gap is input
together with the circuit information. In this case,
the circuit information of the target net includes a
driver, a wiring having a wiring length L = 150 mm
20   and an impedance Z0 = 60 Ohms, a wiring having a
wiring length L = 20 mm and an impedance Z0 = 60
Ohms, and a receiver. The circuit information of
the adjacent net includes a driver, a wiring having
a wiring length L = 100 mm and an impedance Z0 = 70
25   Ohms, a wiring having a wiring length L = 20 mm and
an impedance Z0 = 70 Ohms, and a receiver. In
addition, a pattern gap Gap between the target and
adjacent nets is Gap = 1.27 mm. The step 8 creates
a model of the crosstalk portion when creating the
30   model of the circuit simulator, and obtains the
noise combined waveform by combining the propagation
signal waveform of the target net and the crosstalk
noise waveform output from the circuit simulator.
The noise check is carried out based on the noise
35   combined waveform.

FIG. 13 is a flow chart for explaining a
noise countermeasure determination process of the

CPU 201 of the computer system 100 which is applied
with a sixth embodiment of the noise countermeasure
determination method, a sixth embodiment of the
noise countermeasure determination apparatus and a
5   sixth embodiment of the computer-readable storage
medium according to the present invention. In FIG.
13, those steps which are the same as those
corresponding steps in FIG. 11 are designated by the
same reference numerals, and a description thereof
10   will be omitted. In this sixth embodiment, instead
of inputting the circuit information of the adjacent
net, a simulation model is created by assuming that
a net having the same structure as the target net is
adjacent to the target net with a constant pattern
15   gap formed therebetween.

In FIG. 13, a step 19-1 stores the circuit
information related to the target net, as the
circuit information related to the adjacent net
which is adjacent to the target net, in a storage
20   means such as the memory part 202. In other words,
the circuit information of the adjacent net is
automatically generated by assuming that the net
having the same structure as the target net is
adjacent to the target net with the constant pattern
25   gap formed therebetween. The step 7-1 creates the
simulation models of the target net and the adjacent
net using the circuit information of the adjacent
net.

FIG. 14 is a diagram for explaining the
30   circuit information of the target net and the
adjacent net. As shown in FIG. 14, a crosstalk
portion which should consider the crosstalk is
specified within the net, and the circuit
information of the adjacent net is automatically
35   generated by assuming that the net having the same
structure as the target net is adjacent to the
target net with the constant pattern gap formed

therebetween. In this case, the circuit information of the target net includes a driver, a wiring having a wiring length L = 150 mm and an impedance Z0 = 60 Ohms, a wiring having a wiring length L = 20 mm and

5   an impedance Z0 = 60 Ohms, and a receiver. The circuit information of the adjacent net, which is automatically generated, includes a driver, a wiring having a wiring length L = 150 mm and an impedance Z0 = 60 Ohms, a wiring having a wiring length L = 20

10   mm and an impedance Z0 = 60 Ohms, and a receiver. In addition, a pattern gap Gap between the target and adjacent nets is Gap = 1.27 mm. The step 8 creates a model of the crosstalk portion when creating the model of the circuit simulator, and

15   obtains the noise combined waveform by combining the propagation signal waveform of the target net and the crosstalk noise waveform output from the circuit simulator. The noise check is carried out based on the noise combined waveform.

20   FIG. 15 is a flow chart for explaining a noise countermeasure determination process of the CPU 201 of the computer system 100 which is applied with a seventh embodiment of the noise countermeasure determination method, a seventh

25   embodiment of the noise countermeasure determination apparatus and a seventh embodiment of the computer-readable storage medium according to the present invention. In FIG. 15, those steps which are the same as those corresponding steps in FIG. 13 are

30   designated by the same reference numerals, and a description thereof will be omitted. In this seventh embodiment, the processes from the creation of the simulation model up to the noise check are repeated while changing the pattern gap between the

35   target net and the adjacent net, so as to obtain and output as the noise countermeasures a minimum pattern gap which makes the noise fall within the

tolerable range.

In FIG. 15, a step 7-2 creates a
simulation model based on a maximum value, a minimum
value and a pitch of the pattern gap between the
5   target net and the adjacent net, in addition to the
circuit information of the target net and the
circuit information of the adjacent net. Further, a
step 9-2 creates the circuit information of the
adjacent net using the minimum value of the pattern
10   gap, and carries out a noise check by taking the
crosstalk into consideration. If the noise exceeds
a tolerable range as a result of the noise check,
the pattern gap is increased by an amount
corresponding to the pitch, and the process returns
15   to the step 7-2. Therefore, the steps 7-2, 8 and 9-
2 are repeated until the noise falls within the
tolerable range. Then, a step 21 obtains, as the
noise countermeasures, a minimum pattern gap which
makes the noise fall within the tolerable range. In
20   addition, a step 22 outputs the noise
countermeasures which are obtained.

The processes of each of the embodiments
described above may be carried out based on data of
the circuit design or, data of the assemble design.
25   Moreover, by executing all selectable combinations,
similarly to the noise measure determination method
which outputs the wiring topology as the noise
countermeasures, optimum resistance, branching
length, characteristic impedance of the wiring,
30   wiring pattern width and the like may be output as
the noise countermeasures.

Next, a description will be given of the
recommended circuit information and the noise
countermeasures which are obtained with respect to
35   particular input circuit information. In the
following description, it is assumed for the sake of
convenience that the recommended circuit information

and the noise countermeasures are obtained by the third embodiment shown in FIG. 8.

FIG. 16 is a diagram showing particular input circuit information. In this case, the wiring topology is the load concentration type, and a characteristic impedance Z0 of the wiring pattern is Z0 = 60 Ohms, and a transmission delay time Td of the wiring pattern is Td = 7.0 ns/m. The input circuit information includes a driver DV having an output resistance R0 of R0 = 10 Ohms, a rising time Tr of Tr = 0.7 ns and a falling rime Tf of Tf = 0.6 ns, a wiring having a wiring length L1 of L1 = 150 mm, a wiring having a wiring length L3 of L3 = 30 mm, a wiring having a wiring length L4 of L4 = 100 mm, a receiver RV1 and a receiver RV2.

FIG. 17 is a diagram showing recommended circuit information which is obtained with respect to the input circuit information shown in FIG. 16. In the case of the recommended circuit information shown in FIG. 17, the wiring topology is the load concentration type, and a characteristic impedance Z0 of the wiring pattern is Z0 = 60 Ohms, and a transmission delay time Td of the wiring pattern is Td = 7.0 ns/m. The recommended circuit information includes a driver DV having an output resistance R0 of R0 = 10 Ohms, a rising time Tr of Tr = 0.7 ns and a falling rime Tf of Tf = 0.6 ns, a wiring having a wiring length L2 of L2 = 0 to 35 mm, a damping resistor having a damping resistance Rs of Rs = 40 to 60 Ohms, a wiring having a wiring length L1 of L1 = 150 mm, a wiring having a wiring length L3 of L3 = 0 to 35 mm, a wiring having a wiring length L4 of L4 = 0 to 35 mm, a receiver RV1 and a receiver RV2.

In this case, the recommended value of 40 Ohms $\leq$ Rs $\leq$ 60 Ohms for the damping resistor is calculated from the characteristic impedance Z0 of the wiring and the output resistance R0 of the

driver DV. The recommended value of $0 \leqq L2 \leqq 35$ mm for the wiring length L2 between the driver DV and the damping resistor is calculated from the transmission delay time Td of the wiring pattern and

5   the rising time Tr and the falling time Tf of the driver DV. The recommended value of $0 \leqq L3 \leqq 35$ mm for the wiring length L2 between the branching point and the receiver RV1 is calculated from the transmission delay time Td of the wiring pattern and

10   the rising time Tr and the falling time Tf of the driver DV. The recommended value of $0 \leqq L4 \leqq 35$ mm for the wiring length L4 between the branching point and the receiver RV2 is calculated from the transmission delay time Td of the wiring pattern and

15   the rising time Tr and the falling time Tf of the driver DV.

The noise countermeasures are determined based on differences between the input circuit information shown in FIG. 16 and the recommended

20   circuit information shown in FIG. 17. For example, the noise countermeasures determined in this case include adding a damping resistor Rs having a resistance of 40 to 60 Ohms at a position which is 0 to 35 mm from the driver DV, and changing the wiring

25   length L4 between the branching point and the receiver RV2 to 0 to 35 mm.

FIG. 18 is a diagram showing another particular input circuit information. In this case, the wiring topology is the star type, and a

30   characteristic impedance Z0 of the wiring pattern is Z0 = 60 Ohms, and a transmission delay time Td of the wiring pattern is Td = 7.0 ns/m. The input circuit information includes a driver DV having an output resistance R0 of R0 = 10 Ohms, a rising time

35   Tr of Tr = 0.7 ns and a falling rime Tf of Tf = 0.6 ns, a wiring having a wiring length L1 of L1 = 20 mm, a wiring having a wiring length L2 of L2 = 150 mm, a

wiring having a wiring length L3 of L3 = 150 mm, a receiver RV1 having a load capacitance C1 of C1 = 3 pF, and a receiver RV2 having a load capacitance C2 of C2 = 7 pF.

5   FIG. 19 is a diagram showing recommended circuit information which is obtained with respect to the input circuit information shown in FIG. 18. In the case of the recommended circuit information shown in FIG. 17, the wiring topology is the load

10   concentration type, and a characteristic impedance Z0 of the wiring pattern is Z0 = 60 Ohms, and a transmission delay time Td of the wiring pattern is Td = 7.0 ns/m. The recommended circuit information includes a driver DV having an output resistance R0

15   of R0 = 10 Ohms, a rising time Tr of Tr = 0.7 ns and a falling rime Tf of Tf = 0.6 ns, a wiring having a wiring length L1 of L1 = 0 to 35 mm, a wiring having a wiring length L4 of L4 = 0 to 20 mm, a wiring having a wiring length L5 of L5 = 0 to 20 mm, a

20   damping resistor having a damping resistance Rs1 of Rs1 = 20 to 40 Ohms, a damping resistor having a damping resistance Rs2 of Rs2 = 20 to 40 Ohms, a wiring having a wiring length L2 of L2 = 150 mm, a wiring having a wiring length L3 of L3 = 150 mm, a

25   receiver RV1 having a load capacitance C1 of C1 = 3 pF, and a receiver RV2 having a load capacitance C2 of C2 = 7 pF.

          In this case, the recommended value (maximum value) of Rs1 $\leqq$ 40 Ohms of the first

30   damping resistor and the recommended value (maximum value) of Rs2 $\leqq$ 40 Ohms for the second damping resistor are calculated from the characteristic impedance Z0 of the wiring and the output resistance R0 of the driver DV. In addition, the recommended

35   value (minimum value) of 20 Ohms $\leqq$ Rs1 of the first damping resistor and the recommended value (minimum value) of 20 Ohms $\leqq$ Rs2 for the second damping

resistor are calculated from the load capacitance C1 of the receiver RV1 and the load capacitance C2 of the receiver RV2. The recommended value of $0 \leqq L1 \leqq 35$ mm for the wiring length L1 between the driver
5   DV and the branching point is calculated from the transmission delay time Td of the wiring pattern and the rising time Tr and the falling time Tf of the driver DV. The recommended value of $0 \leqq L4 \leqq 20$ mm for the wiring length L4 between the branching
10 point and the first damping resistor (Rs1) is calculated from the transmission delay time Td of the wiring pattern and the rising time Tr and the falling time Tf of the driver DV. The recommended value of $0 \leqq L5 \leqq 20$ mm for the wiring length L5
15 between the branching point and the second damping resistor (Rs2) is calculated from the transmission delay time Td of the wiring pattern and the rising time Tr and the falling time Tf of the driver DV.

        The noise countermeasures are determined
20 based on differences between the input circuit information shown in FIG. 18 and the recommended circuit information shown in FIG. 19. For example, the noise countermeasures determined in this case include adding a damping resistor Rs1 having a
25 resistance of 20 to 40 Ohms at a position which is between the branching point and the receiver RV1 and is 0 to 35 mm from the branching point, and adding a damping resistor Rs2 having a resistance of 20 to 40 Ohms at a position which is between the branching
30 point and the receiver RV2 and is 0 to 35 mm from the branching point.

        FIG. 20 is a diagram showing still another particular input circuit information. In this case, the wiring topology is the star type, and a
35 characteristic impedance Z0 of the wiring pattern is Z0 = 60 Ohms, and a transmission delay time Td of the wiring pattern is Td = 7.0 ns/m. The input

circuit information includes a driver DV having an output resistance R0 of R0 = 40 Ohms, a rising time Tr of Tr = 0.7 ns and a falling rime Tf of Tf = 0.6 ns, a wiring having a wiring length L1 of L1 = 20 mm,

5   a wiring having a wiring length L2 of L2 = 150 mm, a wiring having a wiring length L3 of L3 = 150 mm, a wiring having a wiring length L4 of L4 = 150 mm, a receiver RV1 having a load capacitance C1 of C1 = 3 pF, a receiver RV2 having a load capacitance C2 of

10   C2 = 3 pF, and a receiver RV3 having a load capacitance C3 of C3 = 4 pF.

     FIG. 21 is a diagram showing recommended circuit information which is obtained with respect to the input circuit information shown in FIG. 20.

15   In the case of the recommended circuit information shown in FIG. 21, the wiring topology is the load concentration type, and a characteristic impedance Z0 of the wiring pattern is Z0 = 60 Ohms, and a transmission delay time Td of the wiring pattern is

20   Td = 7.0 ns/m. The recommended circuit information includes a driver DV having an output resistance R0 of R0 = 40 Ohms, a rising time Tr of Tr = 0.7 ns and a falling rime Tf of Tf = 0.6 ns, a wiring having a wiring length L1 of L1 = 0 to 150 mm, a wiring

25   having a wiring length L2 of L2 = 0 to 55 mm, a wiring having a wiring length L3 of L3 = 0 to 55 mm, a wiring having a wiring length L4 of L4 = 0 to 55 mm, a receiver RV1 having a load capacitance C1 of C1 = 3 pF, a receiver RV2 having a load capacitance

30   C2 of C2 = 3 pF, and a receiver RV3 having a load capacitance C3 of C3 = 4 pF.

     In this case, the load concentration type is selected for the wiring topology, based on the characteristic impedance Z0 of the wiring which is

35   Z0 = 60 Ohms, the output resistance R0 of the driver DV which is D0 = 40 Ohms, the number of receivers which is three in this case, and the load

capacitances C1, C2 and C3 of the receivers RV1, RV2
and RV3 which are C1 = C2 = 3 pF and C3 = 4 pF.   The
recommended value of L1 = 150 mm for the wiring
length L1 between the driver DV and the branching

5   point is calculated from the wiring topology and the
wiring lengths L1, L2 and L3 which are L1 = 20 mm,
L2 = 150 mm and L3 = 150 mm.   The recommended value
of $0 \leq L2 \leq 55$ mm for the wiring length L2 between
the branching point and the receiver RV1 is

10   calculated from the transmission delay time Td of
the wiring pattern and the rising time Tr and the
falling time Tf of the driver DV.   The recommended
value of $0 \leq L3 \leq 55$ mm for the wiring length L3
between the branching point and the receiver RV2 is

15   calculated from the transmission delay time Td of
the wiring pattern and the rising time Tr and the
falling time Tf of the driver DV.   The recommended
value of $0 \leq L4 \leq 55$ mm for the wiring length L4
between the branching point and the receiver RV3 is

20   calculated from the transmission delay time Td of
the wiring pattern and the rising time Tr and the
falling time Tf of the driver DV.

   The noise countermeasures are determined
based on differences between the input circuit

25   information shown in FIG. 20 and the recommended
circuit information shown in FIG. 21.   For example,
the noise countermeasures determined in this case
include changing the wiring topology to the load
concentration type, changing the wiring length L1

30   between the driver DV and the branching point to L1
= 150 mm, changing the wiring length L2 between the
branching point and the receiver RV1 to L2 = 0 to 55
mm, changing the wiring length L3 between the
branching point and the receiver RV2 to L3 = 0 to 55

35   mm, and changing the wiring length L4 between the
branching point and the receiver RV3 to L4 = 0 to 55
mm.

Of course, the recommended circuit information is not limited to the information described above in conjunction with each of the embodiments. For example, the recommended circuit

5 information may include a wiring length between a driver and a damping resistor, wiring lengths between a branching point and each of the receivers, differences between the wiring lengths between the driver and each of the receivers, a resistance of

10 the damping resistor, an inserting position of the damping resistor, a resistance of a pull-up resistor, a resistance of a pull-down resistor, a pull-up voltage, a driving capacity of the driver, a number of loads such as the number of receivers provided

15 with respect to one driver, a wiring topology and the like.

FIG. 22 is a flow chart for explaining a noise countermeasure determination process of the CPU 201 of the computer system 100 which is applied

20 with an eighth embodiment of the noise countermeasure determination method, an eighth embodiment of the noise countermeasure determination apparatus and an eighth embodiment of the computer-readable storage medium according to the present

25 invention. In FIG. 22, those steps which are the same as those corresponding steps in FIG. 4 are designated by the same reference numerals, and a description thereof will be omitted. In this eighth embodiment, a rule check and a topology check are

30 carried out with respect to the input circuit information. When an error is found during the rule check or the topology check, an advice for correcting the error is displayed, so as to reduce the time required to make the circuit correction and

35 to improve the accuracy of the advice.

In FIG. 22, a step 41 carries out a rule check of the circuit (hereinafter simply referred to

as a circuit rule check) with respect to the input
circuit information, and decides whether or not a
rule error is found. The circuit rule check
includes checking a disconnection and a loop (short-
5   circuit) of the wiring, checking the existence of an
antenna wiring, and checking the logic such as
whether or not the circuit consists only of a driver
or only of a receiver, and whether or not no pull-up
resistor is provided in an open-drain circuit. In
10   other words, the circuit rule check makes common and
basic checks of the circuit. As a result, it is
possible to find the rule error of the input circuit
information at an early stage of the noise
countermeasure determination process. If the
15   decision result in the step 41 is YES, a step 42
displays on the display 102 an advice indicating how
the input circuit information should be corrected
with respect to the rule error which is found.
After the step 42, the process returns to the step 1,
20   and the operator corrects the input circuit
information so as to eliminate the rule error
according to the advice.
         On the other hand, if the decision result
in the step 41 is NO, a step 43 carries out a
25   topology check of the wiring (hereinafter simply
referred to as a wiring topology check) with respect
to the input circuit information, and decides
whether or not a topology error is found. The
wiring topology categorizes the wirings of the
30   circuit into how the wirings are connected. The
wiring topology includes the load concentration type
including the 1:1 type, the star type, and the daisy
chain type. For example, it is possible to obtain
good characteristics such as good signal waveforms
35   by employing one of such connection types for the
wirings of the circuit. For this reason, by making
a check to determine the wiring topology employed by

the circuit and finding an erroneous portion which does not conform to the connection type, it is possible to find a topology error of the input circuit information at an early stage of the noise
5 countermeasure determination process. If the decision result in the step 43 is YES, a step 44 displays on the display 102 an advice indicating how the input circuit information should be corrected with respect to the topology error which is found.
10 After the step 44, the process returns to the step 1, and the operator corrects the input circuit information so as to eliminate the topology error according to the advice.

If the decision result in the step 43 is
15 NO, the process advances to the step 3. In other words, when no error is found as a result of the circuit rule check and the wiring topology check which are made with respect to the input circuit information, the recommended circuit information is
20 calculated as in the case of the second embodiment described above based on the checked input circuit information.

Of course, the order in which the steps 41 and 43 are carried out may be reversed. That is, it
25 is possible to carry out the circuit rule check in the step 41 when no topology error exists as a result of the wiring topology check which is carried out in the step 43, and to advance the process to the step 3 when no rule error exists as a result of
30 the circuit rule check.

Therefore, according to this embodiment, it is possible to find the rule error and the topology error at an early stage of the noise countermeasure determination process, as compared to
35 the case where the input circuit information is corrected based on the result of the noise check which is carried out by the waveform analysis or the

like in the step 9, for example. In addition,
because the advice is displayed when one of the rule
error and the topology error is found, it is
possible to reduce the time required to correct the
5 circuit and to improve the accuracy of the advice.

FIG. 23 is a flow chart for explaining a
noise countermeasure determination process of the
CPU 201 of the computer system 100 which is applied
with a ninth embodiment of the noise countermeasure
10 determination method, a ninth embodiment of the
noise countermeasure determination apparatus and a
ninth embodiment of the computer-readable storage
medium according to the present invention. In FIG.
23, those steps which are the same as those
15 corresponding steps in FIG. 22 are designated by the
same reference numerals, and a description thereof
will be omitted. In this ninth embodiment, a rule
check and a topology check are carried out with
respect to the input circuit information. When an
20 error is found during the rule check or the topology
check, an advice for correcting the error is
displayed, so as to reduce the time required to make
the circuit correction and to improve the accuracy
of the advice.

25 In FIG. 23, a step 51 inputs a circuit
diagram and various settings. A step 52 inputs
design conditions, inputs design indexes, specifies
observation points, and specifies check items and
the like. The information input or specified in the
30 step 52 may be made based on CAD data. The steps 51
and 52 correspond to the step 1 shown in FIG. 22,
and input the input circuit information.

A step 53 includes the steps 41 and 42,
and also carries out a portion of the step 3 shown
35 in FIG. 4. Accordingly, the results of the circuit
rule check and the wiring topology check with
respect to the input circuit information are

obtained by the step 53.

A step 54 forms an analyzed net model and a crosstalk model of the input circuit information, based on the results obtained from the step 53, and

5   creates a circuit model therefrom. This step 54 corresponds to the step 7 shown in FIG. 4.

A step 55 includes steps 47, 48 and 49. The step 47 analyzes the created circuit model using a circuit simulator. This step 47 corresponds to

10   the step 8 shown in FIG. 4. The step 48 checks whether or not a noise which will cause a problem, that is, a noise which exceeds a tolerable range, is generated, based on the analysis results of the circuit simulator. Such a noise check may be made

15   based on a signal waveform propagating through a wiring of the electronic circuit and output from the circuit simulator, by detecting a noise existing in the signal waveform. In addition, the step 48 may check the signal waveform analyzed in the step 47,

20   so as to detect a portion which does not conform to the design conditions or an abnormal portion (erroneous portion) in the signal waveform. The step 48 corresponds to the step 9 shown in FIG. 4.

The step 49 categorizes the results of the

25   noise check and optimizes the noise countermeasures, displays the optimized noise countermeasures on the display 102, and displays an advice on the display 102. The step 49 corresponds to the steps 10 and 11 shown in FIG. 4. Accordingly, based on information

30   such as the degree of mismatch of the signal waveform and the design conditions, the kind of abnormality existing in the signal waveform and the voltage and time of the abnormality, the step 49 outputs, as the advice, the analysis results using

35   an advice tree structure. Since an optimum solution for improving the abnormality of the signal waveform is prepared at a tip end of each branch of the

advice tree structure, the optimum solutions with
respect to the various abnormalities, including the
noise, are automatically output as the advice.
After the step 49, the process returns to the step
51, and the operator corrects the circuit depending
on the advice which is output with respect to the
abnormality.

Next, a description will be given of the
judging contents of the rule check made in the step
41 and a corresponding advice made in the step 42.
Of course, the judging contents and the
corresponding advice are not limited to those
described hereinafter. The advice corresponding to
the judging contents is stored in the memory part
202, for example.

If the judging contents are "no floating
element or pattern which is not connected to a
target driver exists", for example, the
corresponding advice output in the step 42 for the
case where the decision result in the step 41 is YES
is "delete floating element or pattern". If the
judging contents are "no loop pattern exists", the
corresponding advice output in the step 42 for the
case where the decision result in the step 41 is YES
is "delete loop". If the judging contents are "no
antenna pattern exists", the corresponding advice
output in the step 42 for the case where the
decision result in the step 41 is YES is "delete
antenna". If the judging contents are "net is not
directly connected to a power source or ground", the
corresponding advice output in the step 42 for the
case where the decision result in the step 41 is YES
is "delete power source or ground directly connected
to the net". If the judging contents are "one or
more receivers exist", the corresponding advice
output in the step 42 for the case where the
decision result in the step 41 is YES is "add

receiver". If the judging contents are "one or more
elements capable of becoming a driver exist", the
corresponding advice output in the step 42 for the
case where the decision result in the step 41 is YES

5   is "add a driver". Furthermore, if the judging
contents are "check number of loads: the recommended
number of loads should be satisfied", the
corresponding advice output in the step 42 for the
case where the decision result in the step 41 is YES

10 is "change to a driver having a larger driving
capacity or, reduce the number of loads to a number
smaller than the recommended number of loads".

        Next, a description will be given of the
judging contents of the topology check made in the

15 step 43 and the corresponding advice made in the
step 44. Of course, the judging contents and the
corresponding advice are not limited to those
described hereinafter. The advice corresponding to
the judging contents is stored in the memory part

20 202, for example.

        FIG. 24 is a diagram showing a load
concentration type wiring topology for a
unidirectional transmission. In the case of such a
load concentration type wiring topology, if the

25 judging contents are "the number of resistors
connected in series is one or less in the case of a
1:1 type unidirectional transmission", the
corresponding advice output in the step 44 for the
case where the decision result in the step 43 is YES

30 is "a damping resistor is redundant if an excess
resistor is connected in series, and thus, maintain
the resistor connected in series closest to a driver
and delete other resistors". In addition, if the
judging contents are "the number of resistors

35 connected in series between a target driver and a
first branching point is one or less in the case of
a 1:1 type unidirectional transmission", the

corresponding advice which is output in the step 44
in the case where the decision result in the step 43
is YES is "a damping resistor is redundant if an
excess resistor is connected in series, and thus,
5   maintain the resistor connected in series closest to
a driver and delete other resistors".

FIGS. 25A and 25B respectively are
diagrams showing a star type wiring topology for the
unidirectional transmission. Both FIGS. 25A and 25B
10   show the star type wiring topologies. In the case
of the start type wiring topologies such as those
shown in FIGS. 25A and 25B, if the judging contents
are "the number of damping resistors after each
branching point is one or less", the corresponding
15   advice output in the step 44 for the case where the
decision result in the step 43 is YES is "match the
number of damping resistors to one if two or more
damping resistors exist after the branching point".

FIGS. 26A and 26B respectively are
20   diagrams showing a daisy chain type wiring topology
for the unidirectional transmission. Both FIGS. 26A
and 26B show the daisy chain type wiring topologies.
In the case of the daisy chain type wiring topology
such as that shown in FIG. 26A, if the judging
25   contents are "the number of damping resistors
between a target driver and a first branching point
is one or less", the corresponding advice output in
the step 44 for the case where the decision result
in the step 43 is YES is "a damping resistor is
30   redundant if an excess resistor is connected in
series, and thus, maintain.the resistor connected in
series closest to a driver and delete other
resistors". In addition, in the case of the daisy
chain type wiring topology such as that shown in FIG.
35   26B, if the judging contents are "a length of a
wiring branching from a main wiring satisfies a
predetermined formula", the corresponding advice

output in the step 44 for the case where the decision result in the step 43 is YES is "make the length of the wiring less than or equal to a predetermined length if the judging contents are not satisfied".

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According to the eighth and ninth embodiments described above, the check is carried out in steps with respect to the input circuit information, and an appropriate advice is output

10 when an error is found. For this reason, it is possible to find the error at an early stage of the noise countermeasure determination process and urge the operator to correct the circuit, thereby efficiently reducing the time required to correct

15 the circuit.

Further, the present invention is not limited to these embodiments, but various variations and modifications may be made without departing from the scope of the present invention.

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